Forward/Backward Annotation Between gEDA/gaf and Pads PowerPCB

Dan McMahill

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1 Forward Annotation of gEDA Schematic Changes to Pads PowerPCB Layout

1.1 Overview

Forward annotation is the process of updating a layout to reflect changes made in the schematic. This process is used when, for example, a new component is added to a schematic and needs to be included in the layout. This section describes how to forward annotate changes in a gEDA schematic to a Pads PowerPCB layout.

Pads implements forward annotation through the use of an ECO (Engineering Change Order) file. The ECO file describes the differences between a current design and the desired design. Pads generates the ECO file by performing a netlist comparison between a new netlist file and the netlist contained in the current layout.

1.2 Detailed Forward Annotation Procedure

This procedure assumes you have a board layout open in Pads and that you have made your schematic changes in `gschem`. For the purposes of illustration, assume your schematic is split into two pages in the files `pg1.sch` and `pg2.sch`.

1. Create an updated Pads netlist by running "`gnetlist -g pads -o mynet.asc pg1.sch pg2.sch`". This will create the netlist file "`mynet.asc`".
2. Make a backup copy of your Pads layout in case things fail in a destructive way.
3. From within Pads, choose the "Tools→Compare Netlist" menu item and choose the following options in the form.

original design to compare:	use current PCB design
new design with changes:	mynet.asc
√	generate differences report
√	generate eco file
comparison options	
√	compare only ECO registered parts
attribute comparison level	
√	ignore all attributes

   Click the OK button to create the ECO file.

4. Examine the ECO file to make sure it looks ok (the ECO file is a text file which can be viewed with any text editor).

5. From within Pads, choose the "File→Import..." menu item. Locate and choose the ECO file created previously.

2 Back Annotation of Pads PowerPCB Layout Changes to gEDA Schematic

Backannotation is the process of updating schematics to reflect changes made in the layout. This process is used, for example, when the reference designators have been renumbered on the layout, when pins have been swapped (e.g. on an AND gate), or slots have been swapped (e.g. on a multi-gate package). This section describes how to backannotate changes in a Pads PowerPCB layout to a gEDA schematic. The Pads PowerPCB tool supports three types of schematic backannotation:

1. Reference designator changes. This is often times used at the end of a layout to give components which are geographically close a set of reference designators which are numerically close.
2. Slot swapping. This is commonly found in digital designs where there may be multiple identical gates in a single package. For example, you may wish to swap which slot is used in a hex inverter.
3. Pin swapping. During layout, the designer may wish to swap equivalent pins on a chip. For example, the two inputs on a NAND gate.

Currently only reference designator changes are automatically processed by the Pads to gschem backannotation tool. The slot and pin swapping changes are provided in a report which the schematic designer must use to manually correct the schematic.

2.1 Detailed Backannotation Procedure

This procedure assumes you have a board layout open in Pads. For the purposes of illustration, assume your schematic is split into two pages in the files `pg1.sch` and `pg2.sch`.

1. Create an up to date Pads netlist by running "`gnetlist -g pads -o mynet.asc pg1.sch pg2.sch`". This will create the netlist file "`mynet.asc`".
2. From within Pads, choose the "Tools→Compare Netlist" menu item and choose the following options in the form.

original design to compare:	mynet.asc
new design with changes:	use current PCB design
$\surd$	generate differences report
$\surd$	generate eco file
comparison options	
$\surd$	compare only ECO registered parts
attribute comparison level	
$\surd$	ignore all attributes

Click the OK button to create the ECO file.

3. Examine the ECO file to make sure it looks ok (the ECO file is a text file which can be viewed with any text editor).

4. Make a backup copy of your gEDA schematic files in case things fail in a destructive way.

5. Run "`pads_backannotate file.eco pg1.sch pg2.sch | tee backanno.log`" where `file.eco` is the name of the ECO file created previously and `pg1.sch` and `pg2.sch` are all of your schematic pages. This will apply the reference designator change portion of the ECO file and also generate a list of pin and slot swapping which must be performed by hand. The file `backanno.log` will contain a log of the session that can be refered to when performing the pin and slot swapping.